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L9 and (row with ((key or comparand) near4 (width or length)))	7

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<u>L10</u>	L9 and (row with ((key or comparand) near4 (width or length)))	7	<u>L10</u>
<u>L9</u>	CAM and ((row or cell or block) near4 (segment\$4 or partition\$4 or section\$4 or split\$4))	7528	<u>L9</u>
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<u>L8</u>	l7 and (row with ((key or comparand) near4 (width or length)))	2	<u>L8</u>
<u>L7</u>	L4 and ((row or cell or block) near4 (segment\$4 or partition\$4 or section\$4 or split\$4))	104	<u>L7</u>
<u>L6</u>	L4 and ((column of row) same (row near4 (segment\$4 or partition\$4 or section\$4 or split\$4)))	0	<u>L6</u>
<u>L5</u>	L4 and column	185	<u>L5</u>
<u>L4</u>	L3 and switch\$3	212	<u>L4</u>
<u>L3</u>	L2 and (CAM near4 (block or cell))	369	<u>L3</u>
<u>L2</u>	compar\$6 near6 row and CAM	995	<u>L2</u>
<u>L1</u>	(((20020126672 or 5619713 or 20030131331 or 6169685 or 6374326 or 5890005).pn.) and (row or column or matrix))	3	<u>L1</u>

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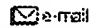
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IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

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Best 200 shown

1 [Pen computing: a technology overview and a vision](#)

André Meyer

July 1995

ACM SIGCHI Bulletin, Volume 27 Issue 3

Full text available:  [pdf\(5.14 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [citations](#), [index terms](#)

This work gives an overview of a new technology that is attracting growing interest in public as well as in industry. The visible difference from other technologies is in the use of a pen or pencil as the primary means of interaction with the machine, picking up the familiar pen and paper interface metaphor. From this follows a set of concepts that are put into context with other emerging technologies and visions. Starting with a short historic ...

2 [Fast detection of communication patterns in distributed executions](#)

Thomas Kunz, Michiel F. H. Seuren

November 1997 **Proceedings of the 1997 conference of the Centre for Advanced Studies on Computer Systems**

Full text available:  [pdf\(4.21 MB\)](#)


Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Understanding distributed applications is a tedious and difficult task. Visualizations based on process execution graphs can obtain a better understanding of the execution of the application. The visualization tool we use is the University of Waterloo. However, these diagrams are often very complex and do not provide a clear overview of the application. In our experience, such tools display repeated occurrences of non-trivial communication patterns.

3 [Scalable high-speed prefix matching](#)

Marcel Waldvogel, George Varghese, Jon Turner, Bernhard Plattner

November 2001 **ACM Transactions on Computer Systems (TOCS)**, Volume 19 Issue 4

Full text available:  [pdf\(933.02 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)


Finding the longest matching prefix from a database of keywords is an old problem with a number of solutions. Dictionary searches to advanced memory management to computational geometry. But perhaps the most common is to use prefix lookups occur in the Internet, when forwarding packets from router to router. Internet traffic is increasing; at the same time, a growing user population is increasing the size of routing tables and the complexity of the forwarding process.

Keywords: collision resolution, forwarding lookups, high-speed networking

4 [Face recognition: A literature survey](#)

W. Zhao, R. Chellappa, P. J. Phillips, A. Rosenfeld

December 2003 **ACM Computing Surveys (CSUR)**, Volume 35 Issue 4

Full text available:  [pdf\(4.28 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)


As one of the most successful applications of image analysis and understanding, face recognition has attracted much attention, especially during the past several years. At least two reasons account for this trend: the first is the commercial and law enforcement applications, and the second is the availability of feasible techniques for face recognition. Even though current machine recognition systems have reached a certain level of maturity, their performance is still far from satisfactory.

Keywords: Face recognition, person identification

5 Special issue: AI in engineering

D. Sriram, R. Joobbani

January 1985 **ACM SIGART Bulletin**, Issue 91

Full text available:  [pdf\(8.79 MB\)](#)

Additional Information: [full citation](#), [abstract](#)

The papers in this special issue were compiled from responses to the announcement in the July 1985 and notices posted over the ARPAnet. The interest being shown in this area is reflected in the six countries. About half the papers were received over the computer network.

6 A pipelined memory architecture for high throughput network processors

Timothy Sherwood, George Varghese, Brad Calder

May 2003 **ACM SIGARCH Computer Architecture News , Proceedings of the 30th annual Computer architecture**, Volume 31 Issue 2

Full text available:  [pdf\(213.66 KB\)](#)


Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)

Designing ASICs for each new generation of backbone routers is a time intensive and fiscally draining on the design of a programmable architecture for backbone routers, based on the manipulation of logic can provide a feasible design alternative to custom ASICs. We propose a pipelined memory design that provides throughput over latency, and co-explore architectural tradeoffs with the design of several important

7 Interactive Editing Systems: Part II

Norman Meyrowitz, Andries van Dam

September 1982 **ACM Computing Surveys (CSUR)**, Volume 14 Issue 3


Full text available:  [pdf\(9.17 MB\)](#)

Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

8 Parallel execution of prolog programs: a survey

Gopal Gupta, Enrico Pontelli, Khayri A.M. Ali, Mats Carlsson, Manuel V. Hermenegildo

July 2001 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 23 Issue 4

Full text available:  [pdf\(1.95 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)

Since the early days of logic programming, researchers in the field realized the potential for exploiting parallel execution of logic programs. Their high-level nature, the presence of nondeterminism, and their rich characteristics, make logic programs interesting candidates for obtaining speedups through parallelism. The fact that the typical applications of logic programming frequently involve irregular computation ...

Keywords: Automatic parallelization, constraint programming, logic programming, parallelism, parallel processing

9 Memory-efficient state lookups with fast updates

Sandeep Sikka, George Varghese

August 2000 **ACM SIGCOMM Computer Communication Review , Proceedings of the conference on Technologies, Architectures, and Protocols for Computer Communication**, Volume 30 Issue 4

Full text available:  [pdf\(384.82 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)

Routers must do a best matching prefix lookup for every packet; solutions for Gigabit speeds are higher, we seek a scalable solution whose speed scales with memory speeds while allowing large lookups. We show that providing such a solution requires careful attention to memory allocation and pipelining on-chip or off-chip SRAM which is limited by either expense ...

10 Design and Implementation of High-Performance Memory Systems for Future Packet Buffer

Jorge García, Jesús Corbal, Llorenç Cerdà, Mateo Valero

December 2003 **Proceedings of the 36th annual IEEE/ACM International Symposium on Microarchitectures**

Full text available:  [pdf\(348.55 KB\)](#)


Additional Information: [full citation](#), [abstract](#), [index terms](#)

In this paper we address the design of a future high-speed router that supports line rates as high as 100 Gbps. Building such a high-speed router would raise many technical challenges, the most important being the packet buffer design, mainly because in router design it is important to provide worst-case performance optimizations. A previous packet buffer design provides worst-case bandwidth guarantees

11 Distributed operating systems

Andrew S. Tanenbaum, Robbert Van Renesse

December 1985 **ACM Computing Surveys (CSUR)**, Volume 17 Issue 4

Full text available:  [pdf\(5.49 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)

Distributed operating systems have many aspects in common with centralized ones, but they also intended as an introduction to distributed operating systems, and especially to current university discussion of what constitutes a distributed operating system and how it is distinguished from a c issues are discussed. Then several examples of current research projects are examined in some d

12 A PDP-8 emulator program

Brian J. Shelburne

March 2002 **Journal on Educational Resources in Computing (JERIC)**, Volume 2 Issue 1

Full text available:  [pdf\(270.03 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)

The clean, simple, and elegant architecture of the classic PDP-8 makes it an ideal candidate for st organization. The PDP-8 emulator program allows a user to write, edit, assemble, debug, trace, a PDP-8 assembler language programs. With it, the user can obtain a feel for the PDP-8. The PDP-8 built-in text editor which is used to write and edit PDP-8 assembler language programs, an assem

Keywords: Computer architecture simulator, education

13 The Vector-Thread Architecture

Ronny Krashinsky, Christopher Batten, Mark Hampton, Steve Gerding, Brian Pharris, Jared Casper, K

March 2004 **ACM SIGARCH Computer Architecture News , Proceedings of the 31st annual Computer architecture ISCA '04**, Volume 32 Issue 2

Full text available:  [pdf\(317.13 KB\)](#)

Additional Information: [full citation](#), [abstract](#)

The vector-thread (VT) architectural paradigm unifies the vectorand multithreaded compute mode programmer with a control processor and a vector of virtualprocessors (VPs). The control process broadcast instructions to all the VPs or each VP can use thread-fetches to direct its own control flo vector and threaded control mechanisms allows a VT architecture to flexibly and compactly encode

14 Applications II: Towards automatic analysis of social interaction patterns in a nursing home e

Datong Chen, Jie Yang, Howard D. Wactlar

October 2004 **Proceedings of the 6th ACM SIGMM international workshop on Multimedia in**

Full text available:  [pdf\(490.67 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [index t](#)


In this paper, we propose an ontology-based approach for analyzing social interaction patterns in interaction patterns are broken into individual activities and behavior events using a multi-level c To take advantage of an ontology in representing how social interactions evolve, we design and r knowledge gained from 80 hours of video recorded in the public spaces of a nursing home. The o

Keywords: human activity, medical care, ontology, social interaction, stochastic modeling

15 On-line Text Editing: A Survey

Andries van Dam, David E. Rice

September 1971 **ACM Computing Surveys (CSUR)**, Volume 3 Issue 3

Full text available:  [pdf\(1.91 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)

This paper is a survey of current methods for the on-line creation and editing of computer program The characteristics of on-line editing systems are examined and examples of various implementat categories: program editors, text editors, and terminals with local editing facilities.

16 String storage and searching for data base applications: Implementation on the INDY backe

George P. Copeland

August 1978 **Proceedings of the fourth workshop on Computer architecture for non-numer**

Full text available:  [pdf\(854.23 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)


User and hardware cost trends dictate that data base systems should provide more complete func

reliability by increasing the amount of hardware present in the system. These goals are accomplished within a one-dimensional cellular storage system called INDY. The INDY backend kernel implementing all data models. The INDY cellular storage array is intended to provide functionality

17 Translator writing systems

Jerome Feldman, David Gries

February 1968 **Communications of the ACM**, Volume 11 Issue 2

Full text available:  [pdf\(4.47 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)

A critical review of recent efforts to automate the writing of translators of programming language: syntax and its application to translator writing are discussed in Section II. Various approaches to (semantic) aspects of translator writing are discussed in Section III, and several related topics in

Keywords: compiler compiler-compiler, generator, macroprocessor, meta-assembler, metacompilation, analysis, syntax, syntax-directed, translator, translator writing system

18 String storage and searching for data base applications: implementation on the INDY backend

George P. Copeland

August 1978 **ACM SIGMOD Record**, **ACM SIGIR Forum**, **ACM SIGARCH Computer Architecture** 2

Full text available:  [pdf\(986.51 KB\)](#)


Additional Information: [full citation](#), [abstract](#), [references](#)

User and hardware cost trends dictate that data base systems should provide more complete functionality by increasing the amount of hardware present in the system. These goals are accomplished within a one-dimensional cellular storage system called INDY. The INDY backend kernel implementing all data models. The INDY cellular storage array is intended to provide functionality

19 Parallel algorithms for data compression

M. E. Gonzalez Smith, J. A. Storer

April 1985 **Journal of the ACM (JACM)**, Volume 32 Issue 2


Full text available:  [pdf\(1.99 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)

Parallel algorithms for data compression by textual substitution that are suitable for VLSI implementation. "dynamic" dictionary schemes are considered.

20 Conference abstracts

January 1977 **Proceedings of the 5th annual ACM computer science conference**

Full text available:  [pdf\(3.14 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [index terms](#)

One problem in computer program testing arises when errors are found and corrected after a program has been tested. How can it be shown that a fix to one area of the code does not adversely affect the execution of the program? A quantitative method for assuring that new program modifications do not introduce new errors into the program is presented. A retest philosophy that every program instruction that could possibly be reached and tested from the start of the program is tested is presented.

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